

## ***MEDIA ALERT***



For more information, contact:

Nanette Collins

Public Relations for SmartDV

[nanette@nvc.com](mailto:nanette@nvc.com)

**SmartDV's TileLink, Verilator VIP on Full Display at RISC-V Summit**  
*VIP Ensures Thorough, Seamless Coverage-Driven Verification Flow Between  
Simulation, Emulation, Formal Verification*

**SAN JOSE, CALIF — December 3, 2019 —**

**WHO:** [SmartDV™ Technologies](#), the ***Proven*** and ***Trusted*** choice for Verification and Design Intellectual Property (IP)

**WHAT:** Will highlight new additions to its extensive and broad portfolio of VIP that support TileLink, the chip-scale interconnect standard, and the Verilator open-source hardware description language (HDL) simulator at the [RISC-V Summit](#). It will offer demonstrations of its Smart ViPDebug™, a visual protocol debugger that reduces debug time.

**WHEN:** Tuesday, December 10, from 11:30 a.m. until 7 p.m. and Wednesday, December 11, from 11:30 a.m. until 4 p.m.

**WHERE:** San Jose Convention Center, San Jose, Calif.

Attendees can schedule Smart ViPDebug demos or meetings to learn how SmartDV's VIP ensures a thorough and seamless coverage-driven verification flow with no

coverage gaps between simulation, emulation or formal verification at [demo@smartdv.com](mailto:demo@smartdv.com).

## About SmartDV

[SmartDV™ Technologies](#) is the **Proven** and **Trusted** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP supports simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services. The result is **Proven** and **Trusted** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit [SmartDV](#) to learn more.

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