SmartDV™

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SmartDV Speeds Delivery of its New CXL Verification IP

First Verification IP Available for New Protocol Based on PCIe Infrastructure

SAN JOSE, CALIF — May 23, 2019 — SmartDV™ Technologies today announced immediate availability of its latest Verification Intellectual Property (IP) to support Compute Express Link (CXL), a new high-speed CPU-to-device and CPU-to-memory interconnect to accelerate the performance of next-generation data centers.

SmartDV, the ***Proven*** and ***Trusted*** choice for Verification IP, is the first Verification IP solutions provider to support the CXL technology based on the industry-proven PCI Express® (PCIe®) infrastructure. CXL Specification 1.0 is an open standard that delivers performance improvements for emerging usage models while supporting an open ecosystem for data center accelerators and other high-speed enhancements.

“CXL is an important new open source standard with the backing of a broad coalition of enterprise computing industry leaders,” remarks Deepak Kumar Tala, managing director SmartDV. “Implementations of CXL are happening and offers us a clear opportunity to be the first to market with a fully verified Verification IP solution for

CXL. Our proprietary SmartDV Compiler and talented engineering group allows us to rapidly bring new Verification IP such as CXL to market quickly."

Delivering SmartDV's CXL Verification IP

SmartDV's CXL Verification IP is fully compliant with revision 1.0 of the CXL Specification and provides a smart way to verify the CXL's bi-directional bus protocol. It is supported by all major verification languages and methodologies, including open verification methodology (OVM), universal verification methodology (UVM) and SystemC.

About CXL

CXL Specification 1.0, ratified by an industry standard group earlier this year, enables a high-speed, efficient interconnect between the CPU and platform enhancements and workload accelerators, such as GPUs, FPGAs and other purpose-built accelerator solutions.

CXL leverages the PCIe 5.0 physical and electrical interface to provide advanced protocols for I/O and memory and coherency interface. It enables memory coherence between the CPU and various accelerators while maintaining a high bandwidth.

SmartDV at Design Automation Conference

SmartDV will feature its CXL Verification IP and its other smart Verification IP solutions at the Design Automation Conference (DAC) in booth #514 Monday, June 3, through Wednesday, June 5, at the Las Vegas Convention Center in Las Vegas, Nev.

DAC attendees can schedule demonstrations through SmartDV's online scheduler.

Pricing and Availability

The SmartDV CXL Verification IP is fully functional and shipping now.

Pricing is available upon request.

About SmartDV

SmartDV™ Technologies is the Proven and Trusted choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Verification and Design IP is compatible with all verification languages, platforms and methodologies supporting all simulation, emulation and formal verification tools used in a coverage-driven chip design verification flow. The result is ***Proven*** *and* ***Trusted*** Verification and Design IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit www.Smart-DV.com to learn more.

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