SmartDV™

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SmartDV Expands Line of Memory Controller Design IP,
Strengthening its Already Broad Portfolio of IP Products
Immediate Availability of HBM2/2E, HBM3, GDDR6, LPDDR4/5 and Flash

SAN JOSE, CALIF. — April 30, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), today released a line of memory controller Design IP used for high-speed memories including HBM2/2E, HBM3, GDDR6 and LPDDR4/5.

It also expanded its support for Flash memory controllers with the additions of Serial Flash, XSPI, and Octal SPI controllers, strengthening its already broad portfolio of Design IP.

"Continuing to expand our portfolio enables us to meet our users' ongoing needs and reinforces our reputation as the proven and trusted choice for Verification and Design IP," remarks Deepak Kumar Tala, SmartDV's managing director. "Our ability to quickly deliver a broad assortment of high-performance memory controller Design IP is a testament to our expertise in ASIC and SoC design and verification as well as the efficiencies of our proprietary compiler."

The new memory controller Design IP offerings are optimized for high performance with low read/write latencies. Area is minimized due to low gates counts and the controllers are designed to work with DFI PHYs as well as integration in FPGA-based designs. In addition, the controllers can support up to 16 AXI slave interfaces with configurable outstanding read/writes.

SmartDV's standard and custom protocol Design IP enables users to get to market quickly and confidently with its proven Design IP cores. A proprietary, automated compiler-based technology enables rapid development and on-demand customization of Design IP compliant with standard interface and communications protocol specifications for new or evolving standards.

The Design IP cores are fast, highly configurable and reusable plug-and-play design solutions for standard interface and communication protocols used in mobile, networking, SoC, automotive, storage, video, memory, mil aero and other applications. SmartDV can rapidly create or customize or design IP based on specific customer demands.

Availability and Pricing

The SmartDV memory controller IP is delivered as soft design IP with register transfer level (RTL) source code and a comprehensive test suite that can be implemented in ASIC, SoC or FPGA designs. Fast turnaround customization is offered also.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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