SmartDV™

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SmartDV Unveils SmartConf Testbench Generator

Automates Handwritten Testbenches for a Variety of Verification Types, Platforms

SAN JOSE, CALIF. — October 6, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification intellectual property (IP), today unveiled SmartConf testbench generator, an add-on automation tool to its extensive Verification IP portfolio.

"Handwritten testbenches are notoriously time consuming and error prone," remarks Deepak Kumar Tala, managing director of SmartDV. "SmartConf automates the process of generating testbenches based on the input configuration set by the user. It generates testbench files for a wide variety of verification types and platforms while saving time and eliminating the tedium that verification engineers typically endure when developing testbenches."

Using SmartConf, verification engineers enter configuration inputs for a target testbench in a graphical user interface. The tool generates the testbench in a chosen language and methodology by the user. The generated testbench is usable immediately or editable per need.

SmartConf generates testbenches in various industry standard languages and methodologies such as Verilog, SystemVerilog, SystemC and UVM with support for various SmartDV Verification IP. They include simulation Verification IP, SimXL™, synthesizable transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or field programmable gate array (FPGA) prototyping platforms, and post-silicon verification IP.

The tool features windows to track lists of IP, settings and configuration, scoreboard/tests and runs that can be saved or retrieved through a restore option. Another option allows users to skip the GUI use model so they can enter a configuration through a configuration file in a text-like format.

It also links directly to SmartDV's ViPDebug™, a visual protocol debugger that streamlines the overall verification and debugging process. SmartDV ViPDebug incorporates in a single window the utilities required in the debugging process, providing visibility and traceability. It can be used with all verification environments and protocols.

SmartConf is available now and works seamlessly with Smart DV's broad portfolio of Verification IP. Pricing and datasheet requests should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Design and Verification IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-

V CPU verification. All of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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