SmartDV™

For more information, contact:
Nanette Collins
Public Relations for SmartDV
(617) 437-1822
nanette@nvc.com

NSITEXE Selects SmartDV TileLink Verification IP for RISC-V Based Applications
Smart TileLink VIP to be Used to Ensure Complete Verification of High-Efficiency, High-Quality Semiconductor IP

SAN JOSE, CALIF — December 10, 2019 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification Intellectual Property (VIP), today announced NSITEXE licensed its TileLink VIP to ensure complete verification of its high-efficiency and high-quality semiconductor IP adaptable to various applications using the RISC-V architecture.

NSITEXE selected SmartDV because it is the only VIP solutions provider to offer a smart way to verify the TileLink fabric and reduce verification time. SmartDV's VIP verifies the TileLink chip-scale interconnect standard, an open-source, high-performance and scalable cache-coherent fabric for RISC-V based or alternative architecture system-on-chip (SoC) designs.

According to Hideki Sugimoto, chief technology officer (CTO) at NSITEXE, Choosing SmartDV's TileLink VIP was a smart decision for its power-efficient data flow processor (DFP) IP used in in-vehicle, industrial applications, and other market

segments. “It accelerated TileLink implementation and verification through faster testbench development.”

“NSITEXE’s mission to contribute to the evolution of next-generation semiconductor technology through its semiconductor IP products neatly aligns with our mission and goals,” remarks Deepak Kumar Tala, SmartDV’s managing director. “We pride ourselves on evolving next-generation SoC designs with our sizable portfolio of standard and custom protocol VIP fully compliant with standard protocol specifications. Users like NSITEXE can verify and debug their designs quickly, easily and more effectively.”

SmartDV will exhibit at the RISC-V Summit today (Tuesday, December 10) from 11:30 a.m. until 7 p.m. and Wednesday, December 11, from 11:30 a.m. until 4 p.m. at the San Jose Convention Center, San Jose, Calif. It will highlight the TileLink VIP and its Verilator VIP, and demonstration its Smart ViPDebug™, a visual protocol debugger that reduces debug time. Attendees can schedule demos or meetings at demo@smart-dv.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP supports simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects

throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit SmartDV to learn more.

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