SmartDV™

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SmartDV's LPDDR5 IP Clocks 612 MHz in FPGA Functional Test, 1.6GHz at 28nm
Outperforms Competition by 3X During Recent Customer Evaluation

SAN JOSE, CALIF. — May 6, 2020 — SmartDV™ Technologies today confirmed its LPDDR5 SDRAM controller design intellectual property (IP) achieved a speed of over 600 megahertz (MHz) in a field programmable gate array (FPGA) functional test and 1.6 gigahertz (GHz) in a 28-nanometer design during a recent competitive evaluation.

The highly configurable LPDDR5 IP scored higher than competitive offerings by delivering faster performance (e.g. clock rate), outperforming the closest competitor by 3X. It demonstrated a smaller footprint due to lower gate count and lower power, as well as lower latency.

"The recent completion of a technical qualification at a large semiconductor company calibrated the performance of our LPDDR5 controller IP and confirmed its exceptional competitive advantage," says Deepak Kumar Tala, SmartDV's managing

director. “We’re especially proud of the IP’s high performance that reached 612Mhz. The closest competitor came in at 200Mhz.”

SmartDV’s design IP targets multiple applications such as high-performance computing, networking, wearables, IoT and mobile, and can be rapidly customized to meet specific user needs. In addition to earlier versions of its LPDDR SDRAM controller IP, it supports the JESD209-5 LPDDR5 protocol standard specification. The IP is compatible with DFI 5.0 and supports a variety of host bust interfaces, including AHB, APB, OCP, TileLink, Wishbone, VCI and Avalon PLB. An open, flexible architecture ensures it can be used for any custom bus interface.

Availability and Pricing

The SmartDV LPDDR5 controller IP is delivered as soft design IP with register transfer level (RTL) source code and a comprehensive test suite that can be implemented in ASIC, system-on-chip (SoC) or FPGA designs.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly

customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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