NEWS RELEASE

SmartDV™

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SmartDV Announces Support for ARINC Standards with Design and Verification IP

High-Quality, Highly Configurable Design and Verification IP Compliant with Avionics Standards

SAN JOSE, CALIF. — June 3, 2021 — SmartDV™ Technologies, the leader in Design and Verification Intellectual Property (IP), today announced support of the ARINC standards with its Design and Verification IP.

ARINC standards describe avionics, cabin systems, protocols and interfaces used by air transport and business aircraft. Currently, SmartDV's Design IP is compliant with the ARINC 664 standard. Its Verification IP is compliant with ARINC 419, 429, 664, 818 and 825 standards.

"Engineers designing avionics equipment without exception require high-quality Design and Verification IP," notes Deepak Kumar Tala, managing director of SmartDV. "When they partner with SmartDV, they can be assured of a complete IP solution for their design and verification needs backed by an experienced R&D team and exceptional customer support."

Design IP

SmartDV's high-quality, highly configurable and silicon-proven Design IP is pre-verified and delivered in Verilog source code. The comprehensive solution includes lint, clock domain crossing, synthesis, simulation scripts with waiver files and documentation.

Verification IP

An extensive Verification IP portfolio offered by SmartDV is used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects to verify and debug designs quickly, easily and more effectively. The Verification IP is compatible with all verification languages, platforms and methodologies supporting all simulation, emulation and formal verification tools used in a coverage-driven chip design verification flow.

SmartDV's proprietary, automated compiler-based technology ensures quick delivery of its offerings compliant with ARINC standards and other protocol specifications for new or evolving applications. It also comes with SmartDV's Automation Tool Suite that provides rapid testbench generation and visual protocol debugging.

Availability and Pricing

The SmartDV Design and Verification IP portfolio for ARINC standards is available now.

Pricing is available upon request.

Email requests for more information should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies offers the largest portfolio of Design and Verification Intellectual Property (IP) used by more than 200 customers worldwide, including seven of the top 10 semiconductor companies and four of the largest consumer electronics companies. It supports market segments and protocols as diverse as mobile and 5G, networking and SoC, automotive and serial bus, storage, video and defense and aerospace. With more than 600 products in its portfolio, SmartDV covers the design flow with Design IP and Verification IP for use in simulation, emulation, formal and post-silicon validation and memory modeling. SmartDV has the best customer service with more than 250 experienced ASIC and SoC design and verification engineers, a global footprint and local sales offices. Its technical support is available 24 hours a day seven days a week. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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