

Key Benefits

- Saves time by automating the testbench creation process
- Reduces errors by eliminating the need for handwritten testbenches
- Flexible — supports industry-standard verification languages and methodologies
- Graphical User Interface for managing inputs and configuration settings
- Links directly to SmartViPDebug, SmartDV's visual protocol debugger

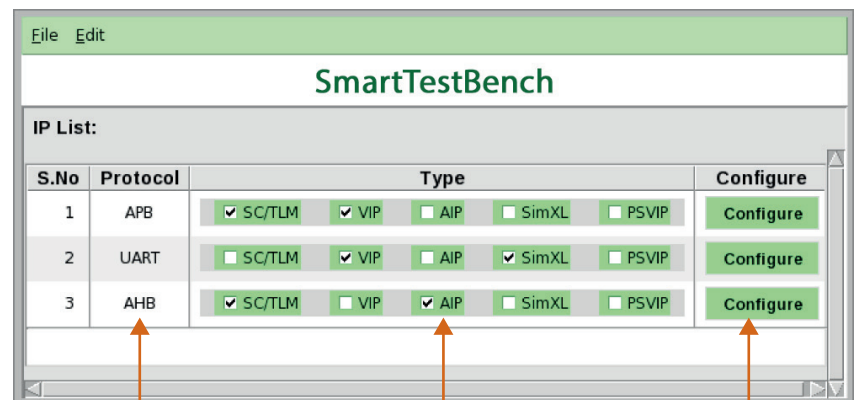
Product Features

- Streamlines and simplifies the protocol debugging process
- Compatible with all SmartDV Verification IP products
- Input and control via user choice of intuitive GUI or text-based configuration files
- Generated testbenches are fully editable
- Usage model spans simulation, emulation, formal and post-silicon verification

SmartTestBench™

SmartTestBench™ automates the creation of testbenches and removes the need for tedious, time-consuming and often error-prone handwritten testbenches. Testbenches can be automatically generated in various industry-standard languages and methodologies including Verilog, SystemVerilog, SystemC and UVM. They support SmartDV Verification IP, SimXL™ (synthesizable transactors for accelerating emulation and FPGA prototyping), assertion-based (formal) verification and post-silicon verification IP.

SmartTestBench features windows to track lists of IP, settings and configuration, scoreboard/tests and runs that can be saved or retrieved through a restore option. Users may also interact with SmartTestBench via a text-based configuration file if they prefer not to use the Graphical User Interface (GUI) mode. The tool links directly to SmartViPDebug, a visual protocol debugger offered by SmartDV that streamlines the verification and debugging process.



List of protocols added

Select protocol types

Configure IP products

General Use Model

Inputs to SmartTestBench can be driven through the provided GUI or via text-based configuration files. The user inputs a list of the protocols to be included, the type of protocol—VIP, SimXL, Assertion IP, etc.—and configuration data for the IP products. The tool then generates the testbench in the chosen language and methodology specified by the user.

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SmartDV™

The Leader in Design and Verification IP

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